

U.S. Department of Commerce, Patent and Trademark Office		Attorney Docket No.	Serial No.				
		SUN030009	10/694,139				
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use several sheets if necessary)</i>		Applicant(s)					
<i>MAY 13 2004</i>		Tong Xiao et al.					
		Filing Date	Group				
		October 27, 2003	2183 2825				
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
AA							
AB							
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AE							
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AG							
AH							
Foreign Patent Documents							
		Document	Date	Country	Class	Subclass	Translation
	AJ						<input type="checkbox"/> <input type="checkbox"/>
	AK						<input type="checkbox"/> <input type="checkbox"/>
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
SM	AL	Ajay J. Daga, Loa Mize, Subramanyan Sripada, Chris Wolff and Quiyang Wu "Automated Timing Model Generation" Synopsys, Inc. DAC 2002, June 2002					
SM	AM	Noriya Kobayashi and Sharad Malik "Delay Abstraction in Combinational Logic Circuits" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pages 1205-1212, Volume 16, Issue 10, October 1997					
SM	AN	Clayton B. McDonald and Randal E. Bryant "A Symbolic Simulation-Based Methodology for Generating Black-Box Timing Models of Custom Macrocells" IEEE, Proceedings of the 2001 International Conference on Computer Aided Design, November 2001					
SM	AO	S.V. Venkatesh, Robert Palermo, Mohammad Mortazavi, and Karem A. Sakallah "Timing Abstraction of Intellectual Property Blocks" IEEE 1997 Customer Integrated Circuits Conference, Pages 99-102, 1997					
SM	AP	Hakan Yalcin, Mohammad Mortazavi, Robert Palermo, Cyrus Bamji and Karem Sakallah "Functional Timing Analysis for IP Characterization" Design Automation Conference, June 1999					
	AQ						
Examiner	/Suresh Memula/		Date Considered	08/26/2006			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
		AL					<input type="checkbox"/>	<input type="checkbox"/>
		A					<input type="checkbox"/>	<input type="checkbox"/>
		AN					<input type="checkbox"/>	<input type="checkbox"/>
		AO						
		AP						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
SM	AR	Moon, Cho W.; Kriplani, Harish; Belkhale, Krishna P. "Timing Model Extraction of Hierarchical Blocks by Graph Reduction" IEEE/ACM Proceedings of the 2002 Design Automation Conference, June 2002					
SM	AS	Yalcin, Hakan; Mortazavi, Mohammad; Bamji, Cyrus; Sakallah, Karem A. "Fast and Accurate Timing Characterization Using Functional Information" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 20, Number 2, February 2001					
SM	AT						

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